NEC

MOS FIELD EFFECT TRANSISTOR
2SK3483

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

DESCRIPTION

The 2SK3483 is N-Channel MOS Field Effect Transistor designed for high current switching applications.

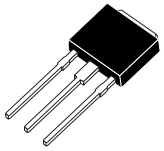
ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3483	TO-251
2SK3483-Z	TO-252

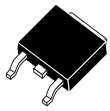
FEATURES

- Low On-State Resistance
  $R_{DS(on)1}$ = 46 mΩ MAX. (V_{GS} = 10 V, I_D = 14 A)
  $R_{DS(on)2}$ = 53 mΩ MAX. (V_{GS} = 4.5 V, I_D = 14 A)
- Low C_{iss} : C_{iss} = 2300 pF TYP.
- Built-in Gate Protection Diode
- TO-251/TO-252 package

(TO-251)



(TO-252)



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage	V_{DSS}	100	V
Gate to Source Voltage	V_{GSS}	±20	V
Drain Current (DC)	$I_{D(DC)}$	±28	A
Drain Current (Pulse) Note1	$I_{D(pulse)}$	±112	A
Total Power Dissipation (T_C = 25°C)	P_T	40	W
Total Power Dissipation (T_A = 25°C)	P_T	1.0	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C
Single Avalanche Current Note2	I_{AS}	T.B.D. Note3	A
Single Avalanche Energy Note2	E_{AS}	T.B.D. Note3	mJ

Notes 1. PW ≤ 10 μs, Duty cycle ≤ 1%

2. Starting T_{ch} = 25°C, R_G = 25 Ω, V_{GS} = 20 V → 0 V

3. T.B.D. : To be determined

THERMAL RESISTANCE

Channel to Case	$R_{th(ch-C)}$	3.13	°C/W
Channel to Ambient	$R_{th(ch-A)}$	125	°C/W

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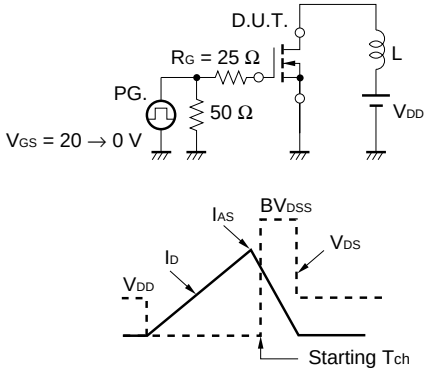
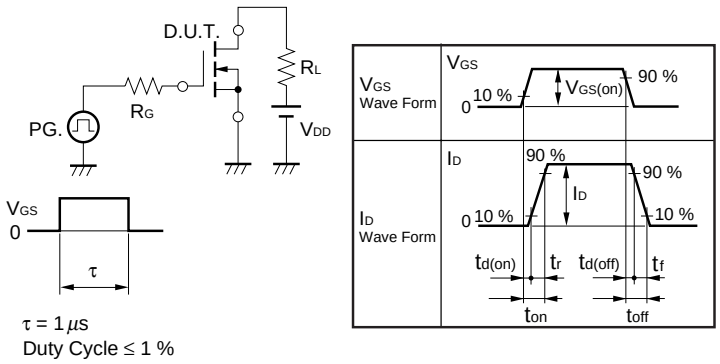
ELECTRICAL CHARACTERISTICS (T_A = 25°C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 14 A		36	46	mΩ
	$R_{DS(on)2}$	V_{GS} = 4.5 V, I_D = 14 A		39	53	mΩ
Gate to Source Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS} = 10 V, I_D = 14 A	16	32		S
Drain Leakage Current	I_{DSS}	V_{DS} = 100 V, V_{GS} = 0 V			10	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±10	μA
Input Capacitance	C_{iss}	V_{DS} = 10 V		2300		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		230		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		120		pF
Turn-on Delay Time	$t_{d(on)}$	I_D = 14 A		17		ns
Rise Time	t_r	$V_{GS(on)}$ = 10 V		10		ns
Turn-off Delay Time	$t_{d(off)}$	V_{DD} = 50 V		55		ns
Fall Time	t_f	R_G = 1 Ω		9.0		ns
Total Gate Charge	Q_G	I_D = 28 A		42		nC
Gate to Source Charge	Q_{GS}	V_{DD} = 80 V		7.0		nC
Gate to Drain Charge	Q_{GD}	$V_{GS(on)}$ = 10 V		12		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	I_F = 28 A, V_{GS} = 0 V		1.0		V
Reverse Recovery Time	t_{rr}	I_F = 28 A, V_{GS} = 0 V		88		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		170		nC

TEST CIRCUIT 1 AVALANCHE CAPABILITY

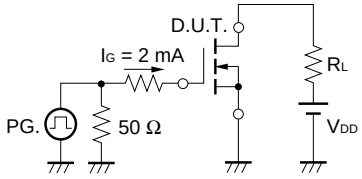


TEST CIRCUIT 2 SWITCHING TIME



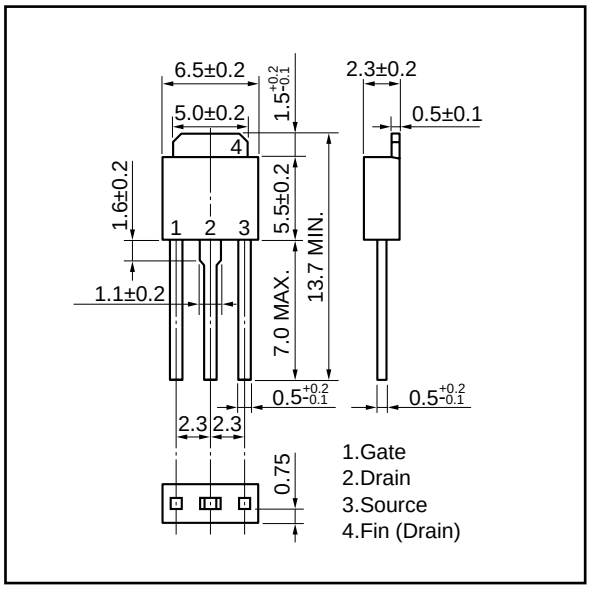
τ = 1 μs
Duty Cycle ≤ 1 %

TEST CIRCUIT 3 GATE CHARGE

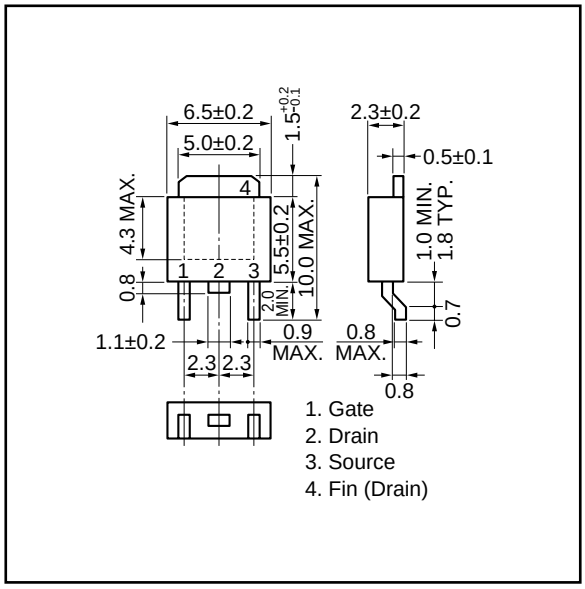


PACKAGE DRAWINGS (Unit : mm)

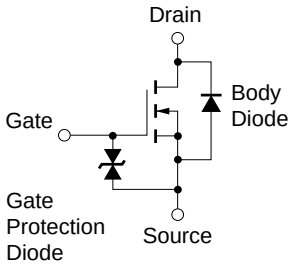
1) TO-251 (MP-3)



2) TO-252 (MP-3Z)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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